

Blackmore Product Brief

11G OTU2 with (Enhanced) Forward Error Correction

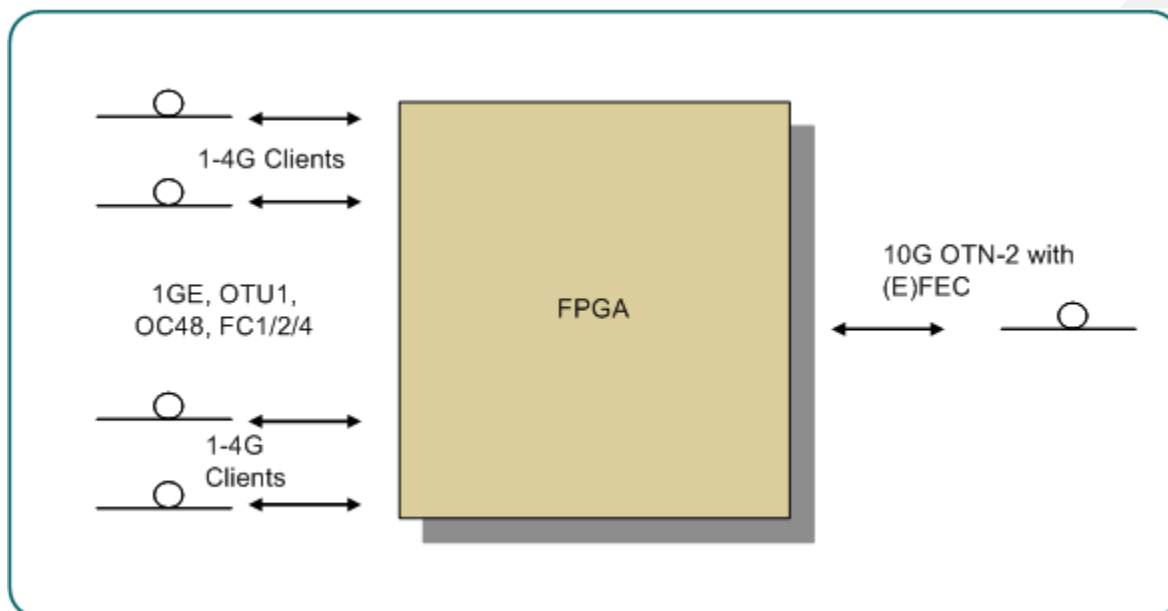
Features:

- SFI4.1 connects to 10G optical transponders
- 10.7G throughput
- Optional G.709 FEC or Enhanced FEC Encoding and Decoding
- Compliant with ITU-T G.709 and ITU-T G.798 recommendations
- Extensive packet and OTU2 statistics
- Generic CPU interface for control and monitoring
- Digital Core suitable for both FPGA and ASIC implementations
- Supports one OTU2/STM-64 stream via a standard OIF SFI-4 interface for direct connection to SERDES
- Can be combined with various SONET / SDH configurations
- Client side can support a variety of combinations of 1GE, OTU1, STM16 / STS48

Key Benefits

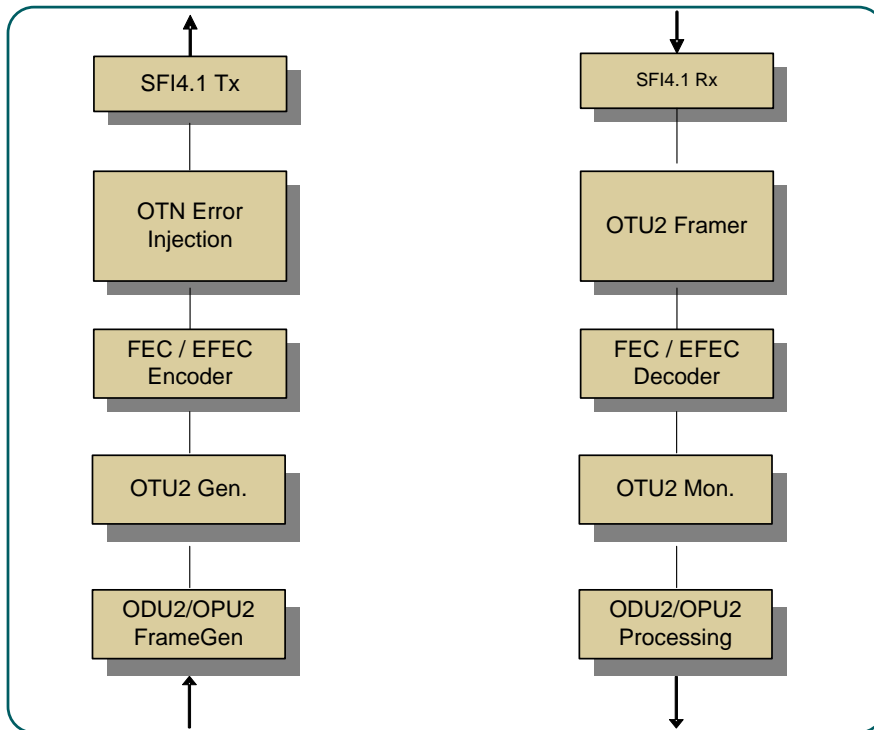
- Core is customized per customer using internal IP library
- Choice of Enhanced FEC or G.709 FEC
- Flexible core allows for use of your line card in multiple applications
- Optional SONET/SDH Support

Example Application: 10G Multiprotocol Muxponder





Block Diagram



Standards Support:

- Framing
 - FAS - The Blackmore uses a Frame Alignment Signal to frame up and to identify OOF and LOF conditions
 - MFAS – The Blackmore supports a multi-frame structure via a Multi-frame alignment signal byte
- OTU2 Section Overhead Monitoring
 - Trail Trace Identifier (TTI) Monitoring
 - BIP-8
 - BEI / BIAE Monitoring
 - Backward Defect Indicator (BDI) Monitoring
 - Incoming Alignment Error (IAE) Monitoring
- ODU2 Path Overhead Monitoring
 - Trail Trace Identifier (TTI) Monitoring
 - BIP-8
 - Backward Detect Indication (BDI)
 - Backward Error Indication (BEI)
 - AIS Maintenance Signal Detection
 - OCI Maintenance Signal Detection
 - Tandem Connection Monitoring (TCM)
 - LCK Maintenance Signal Detection
- OPU2 Overhead
 - Adds support for various client signals
 - Payload Structure Identifier (PSI)
 - Payload Type (PT)
 - Multiplex Structure Identifier
 - Justification Control



Product Overview

In the egress direction, data is first received on the selected client interface (LVDS for example). The Blackmore core performs SM/TCMi/PM BIP-8 parity calculation and insertion, OTU2/ODU2/OPU2 overhead insertion, RS(255,239) FEC encoding and scrambling or EFEC encoding. Overhead can be inserted from an external port or through internal register programming. The OTU2 frames are sent out SFI4 that connects to an optical module.

Alternatively, GFP can be used to map a client signal. The GFP block conforms to the GFP standard, G.7041. The selectable frame formats are Frame Mapped or Transparent Ethernet, Framed Mapped PPP, Transparent Fibre Channel, and Transparent Digital Video (DVB ASI), with other formats available on a per-need basis. These GFP frames are then mapped into the OTU-2 payload area for transport.

In the ingress direction, the OTU2 block byte aligns incoming data, de-scrambles appropriate frame byte locations, performs RS(255,239) FEC decoding and error correction, detects error conditions, accumulates various condition counts, and extracts OTU2/ODU2/OPU2 overhead information to both internal register locations and external overhead ports.

If GFP is used, the GFP blocks are then decoding into one of Ethernet, PPP, Fibre Channel, or Digital Video, with other formats possible on a per-need basis. These blocks use steered to the chosen client side interface.

The client side datapath runs at 155 MHz, at a data width of 256 bits. The line side datapath runs at the expanded OTU2 rate, 170 MHz.

The Blackmore supports a line rate of 10.75 Gb/s and can be over-clocked to support higher data rates.

Forward Error Correction

Avalon's Blackmore core can be configured with G.709 Forward Error Correction or Enhanced Forward Error Correction. G.709 FEC is a Reed-Solomon RS(255,239) based algorithm with approximately 6dB of coding gain. EFEC alternatives include ITU standards based codes and alternative proprietary codes. Avalon offers a variety of choices for Enhanced FEC including standards based FEC algorithms with more than 8dB of coding gain. Avalon's FEC codes support over-clocked rates.

Customization & Support

Using an extensive Internal IP library, Avalon can build a complete Field Programmable Standard Product (FPSP) – a complete FPGA based solution developed to a custom functional specification. By making use of hardware validated IP cores, Avalon can deliver a custom, validated, field programmable solution at lightning speed.

In addition to product customization, Avalon can provide any necessary software drivers to support our products.

Avalon will provide the necessary support to aid in getting your product up and running. In addition to our design and verification environment, Avalon provides telephone and email support as well as on-site field support.

Contact

Please contact Avalon by phone or at the following:

info@avalonmicro.ca